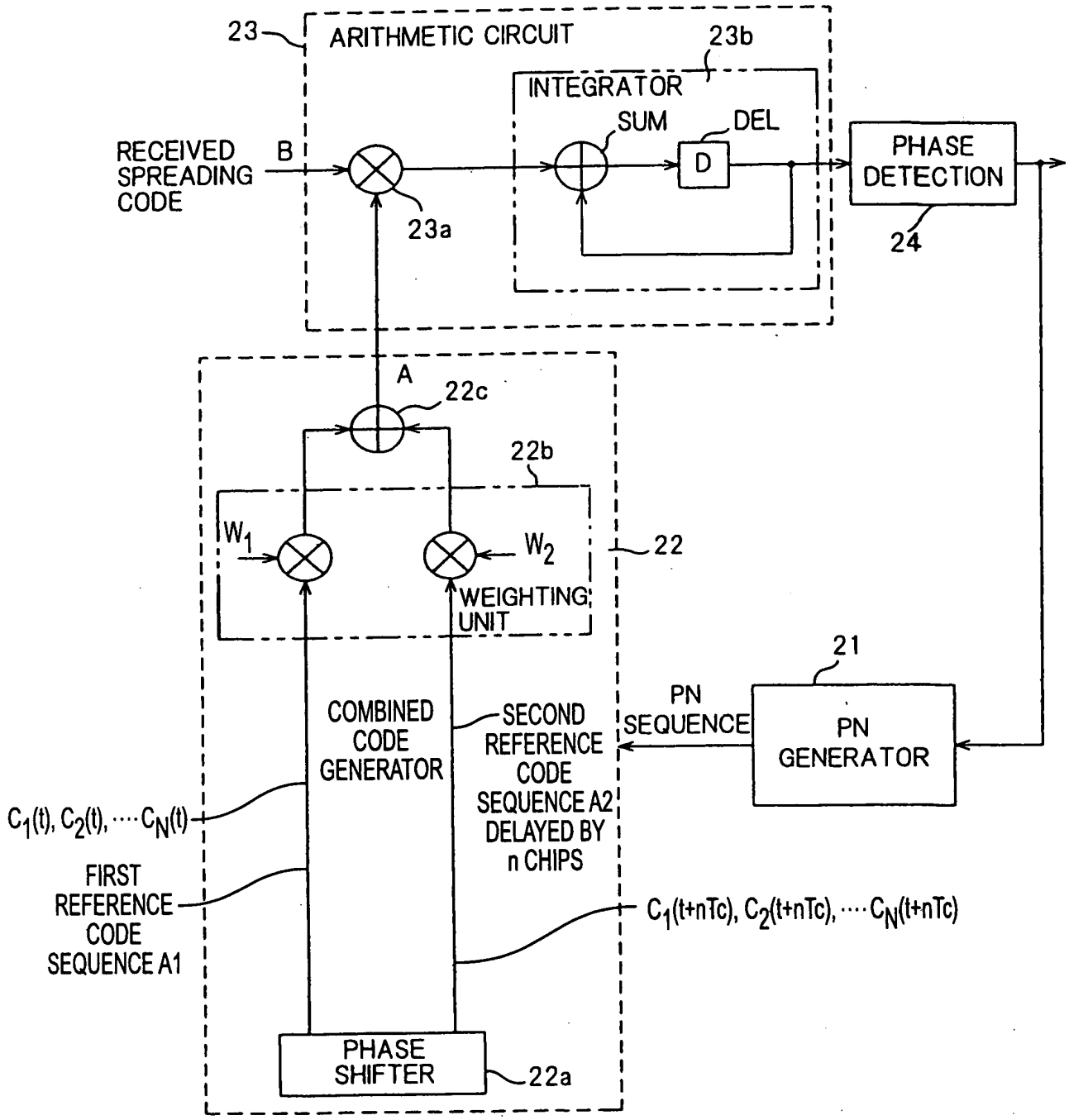

FIG. 1

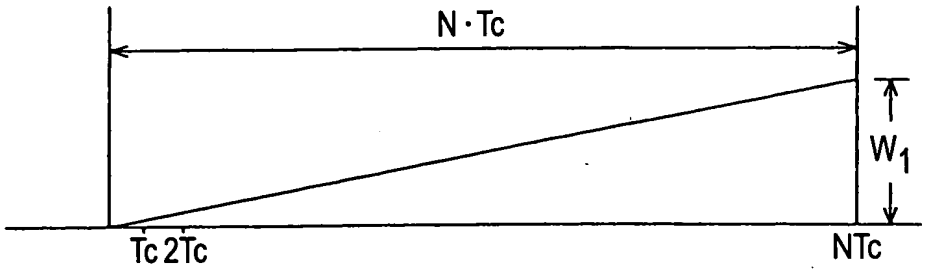

FIG. 2a

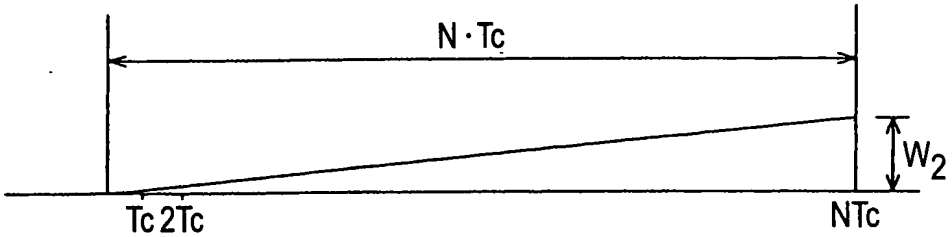

FIG. 2b

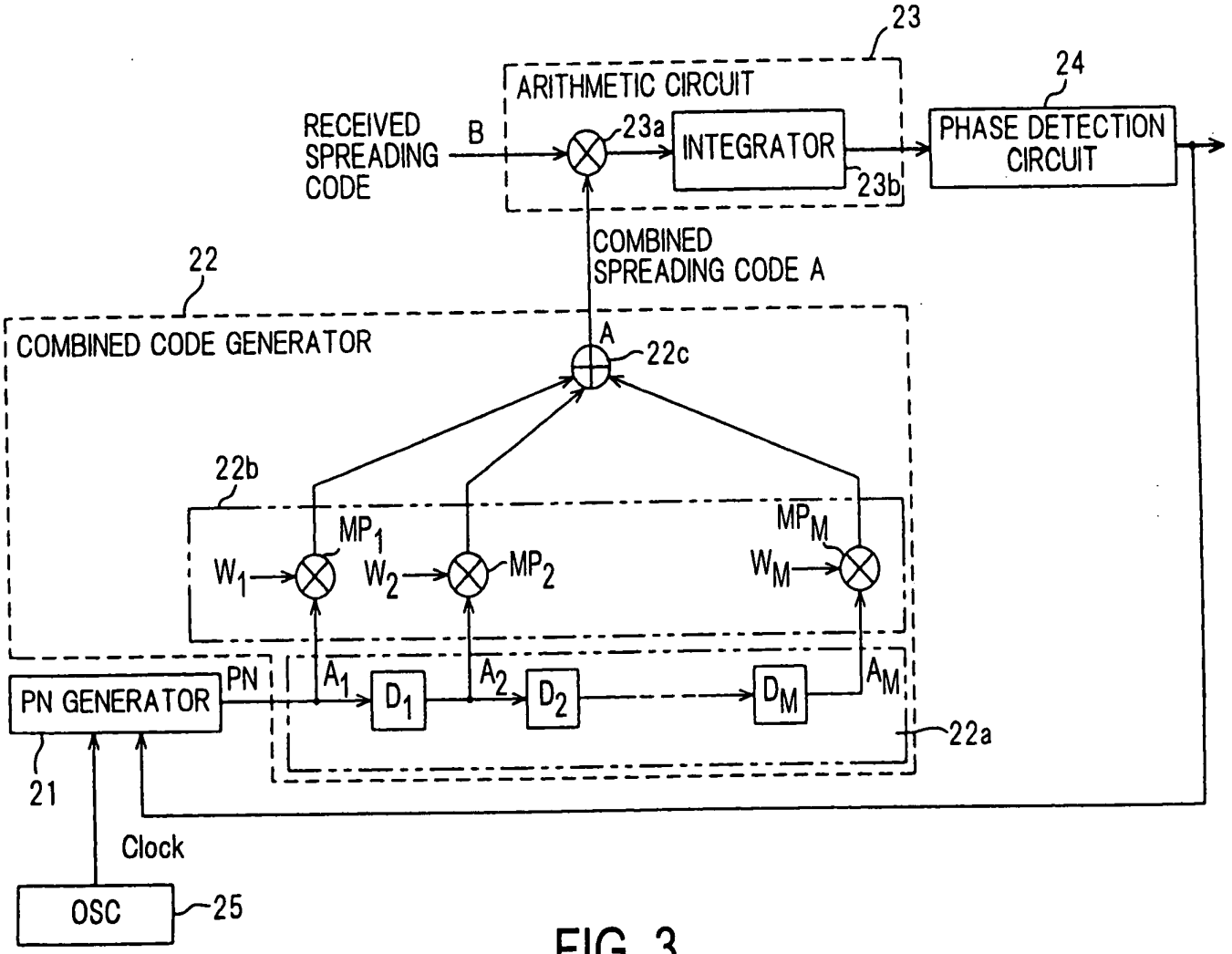
23
ARITHMETIC CIRCUIT
24
RECEIVED SPREADING CODE
B
23a
INTEGRATOR
23b
PHASE DETECTION CIRCUIT
COMBINED SPREADING CODE A
22
COMBINED CODE GENERATOR
A
22c
22b
MP1
MPM
W1
W2
MP2
WM
PN GENERATOR
PN
A1
D1
A2
D2
DM
AM
22a
21
Clock
OSC
25

FIG. 3

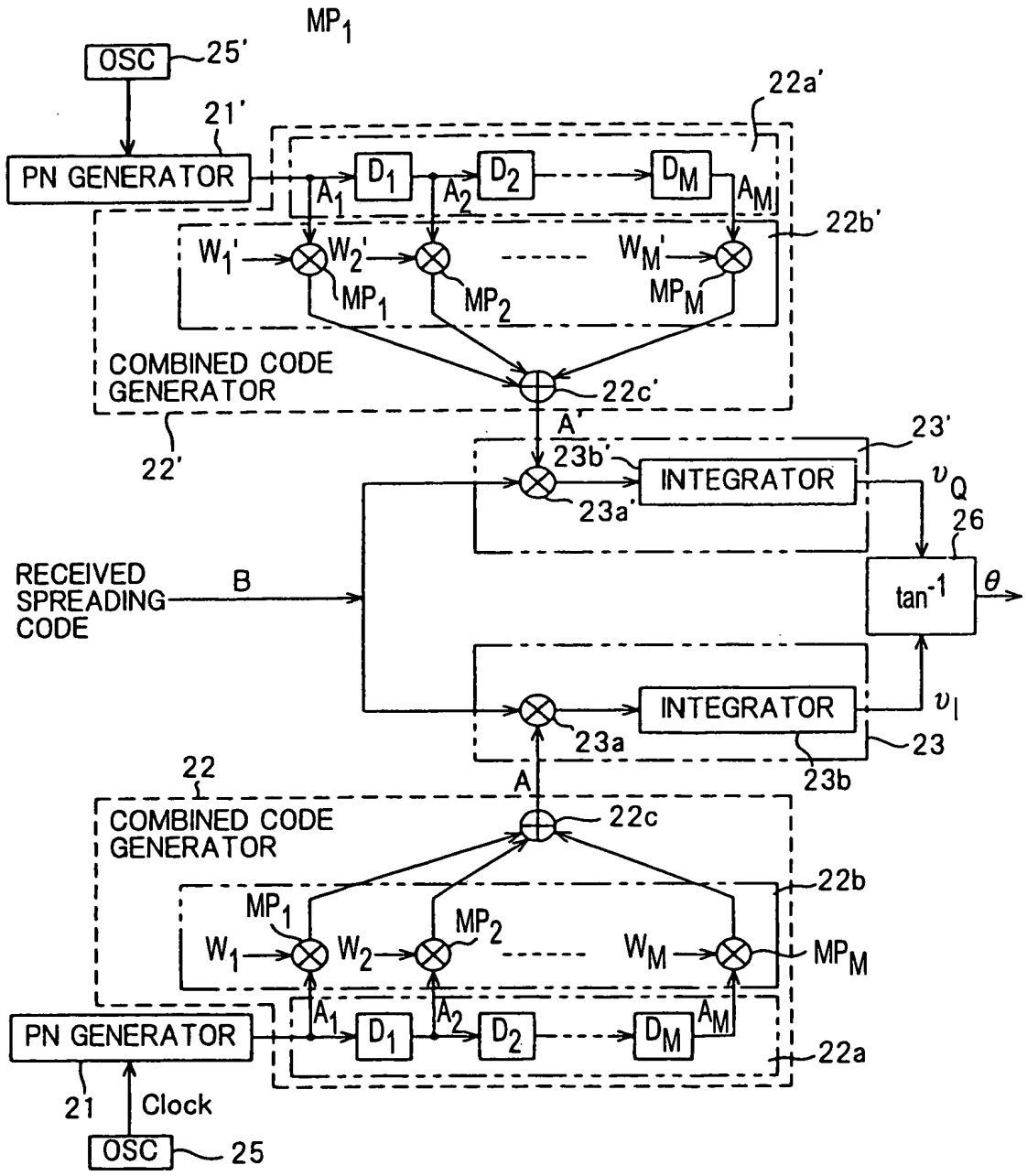
MP1
OSC
25'
21'
22a'
PN GENERATOR
D1
D2
DM
A1
A2
AM
22b'
W1'
W2'
WM'
MP1
MP2
MPM
COMBINED CODE GENERATOR
22c'
22'
A'
23'
23b'
INTEGRATOR
υQ
23a'
26
RECEIVED SPREADING CODE
B
tan-1
θ
INTEGRATOR
υI
23a
23
23b
22
A
COMBINED CODE GENERATOR
22c
22b
MP1
MP2
W1
W2
WM
MPM
A1
A2
AM
PN GENERATOR
D1
D2
DM
22a
21
Clock
OSC
25

FIG. 4

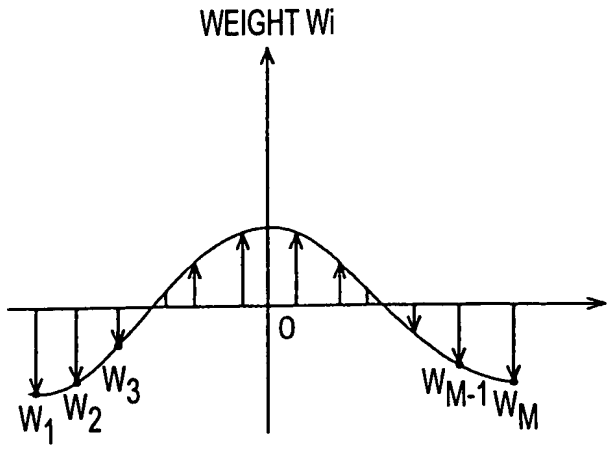

FIG. 5a

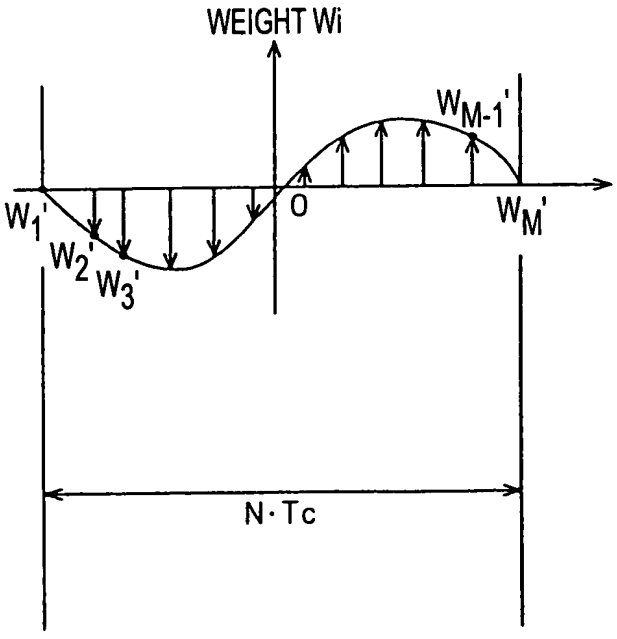

FIG. 5b

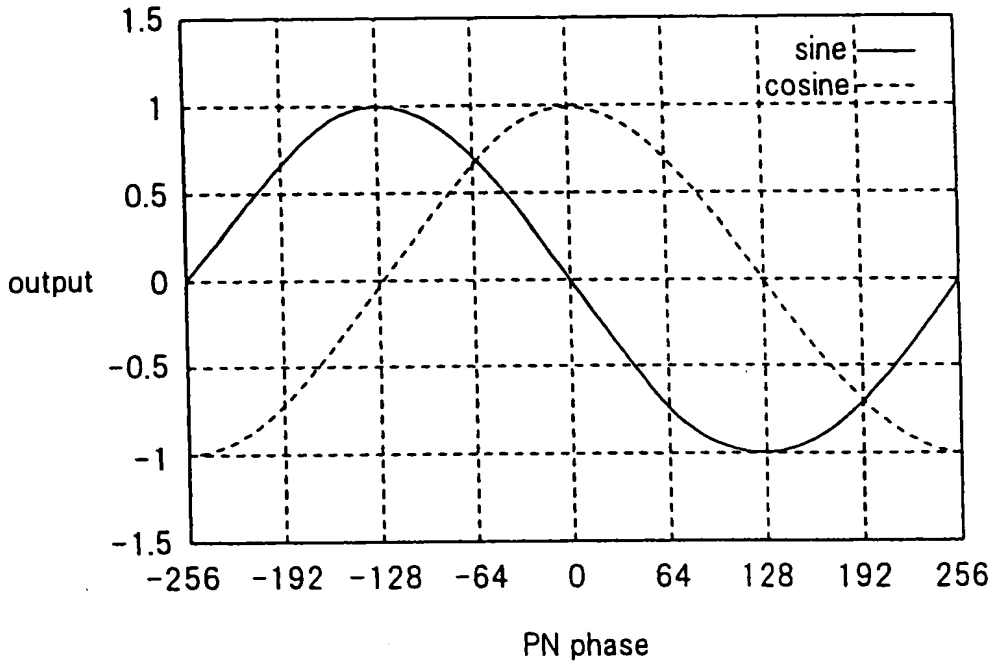
1.5
1
0.5
0
-0.5
-1
-1.5
output
sine
cosine
-256
-192
-128
-64
0
64
128
192
256
PN phase

FIG. 6

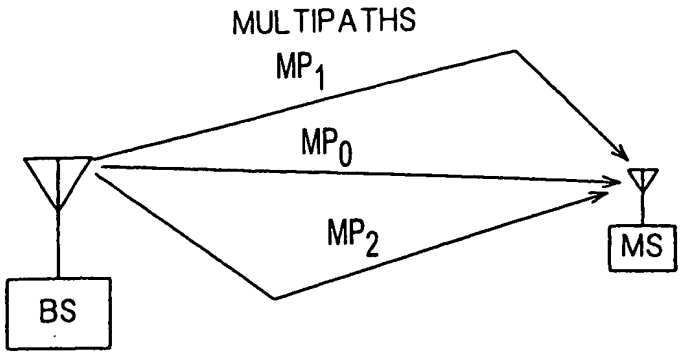

FIG. 7a

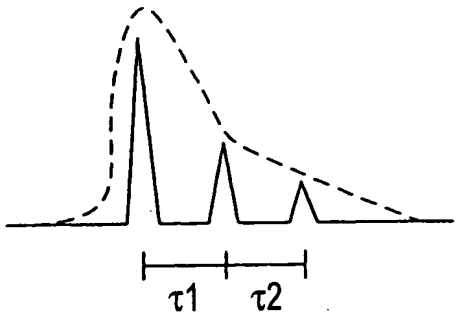

FIG. 7b

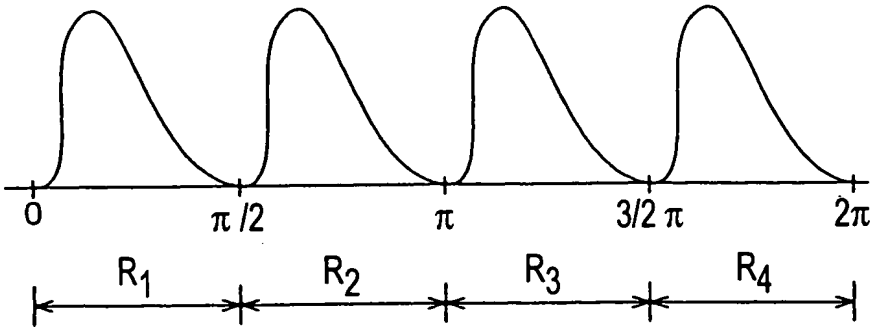

FIG. 7c

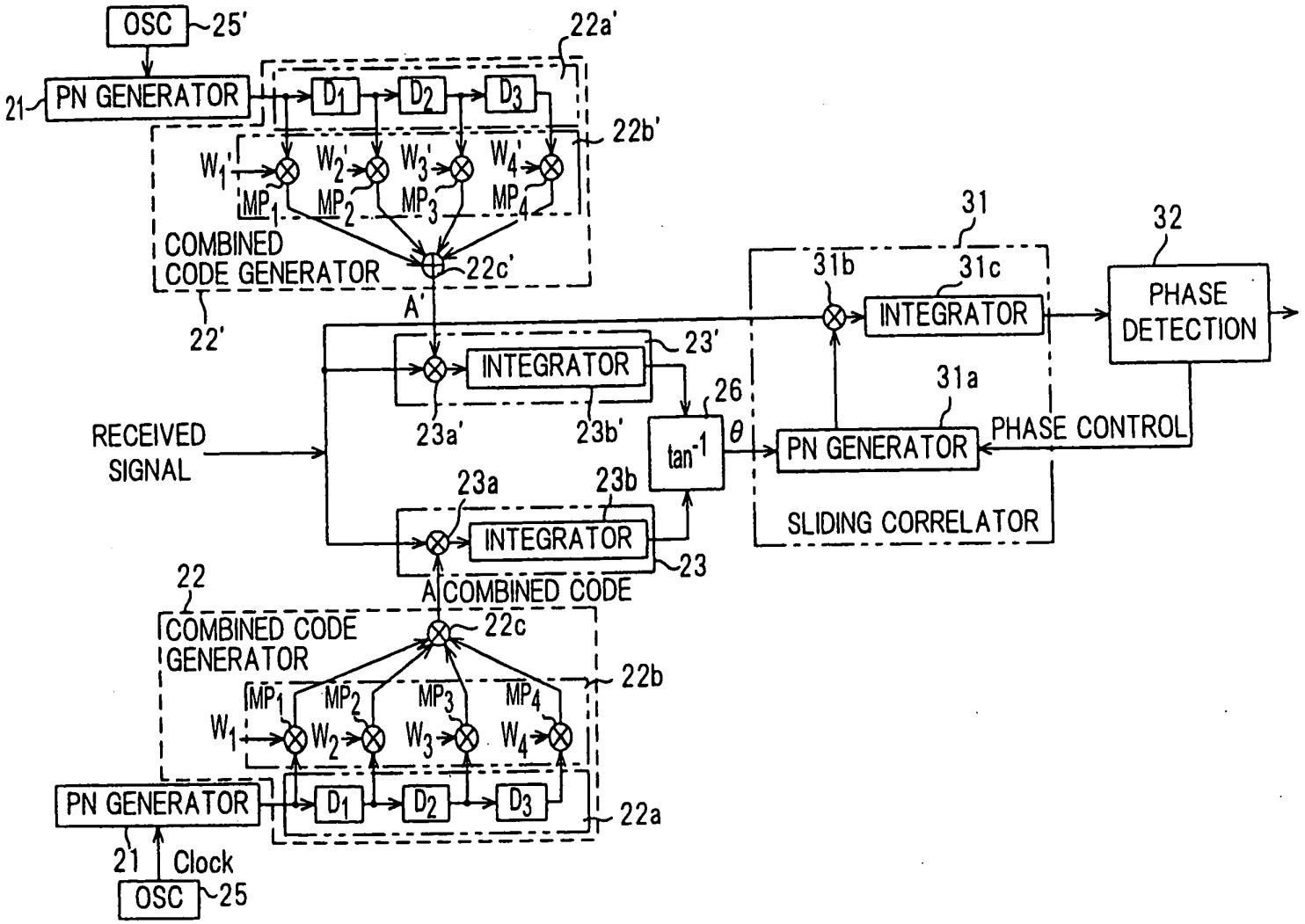
OSC
25'
22a'
21
PN GENERATOR
D1
D2
D3
22b'
W1'
W2'
W3'
W4'
MP1
MP2
MP3
MP4
COMBINED CODE GENERATOR
22c'
22'
A'
31
31b
31c
INTEGRATOR
32
PHASE DETECTION
23'
INTEGRATOR
26
31a
RECEIVED SIGNAL
23a'
23b'
tan-1
θ
PN GENERATOR
PHASE CONTROL
23a
23b
INTEGRATOR
SLIDING CORRELATOR
23
22
A COMBINED CODE
COMBINED CODE GENERATOR
22c
22b
MP1
MP2
MP3
MP4
W1
W2
W3
W4
PN GENERATOR
D1
D2
D3
22a
21
Clock
OSC
25

FIG. 8

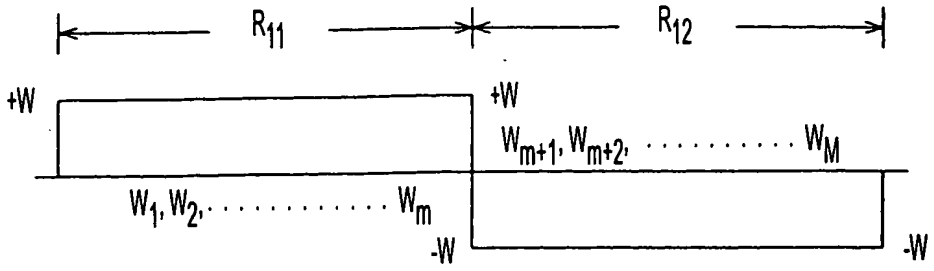

FIG. 9a

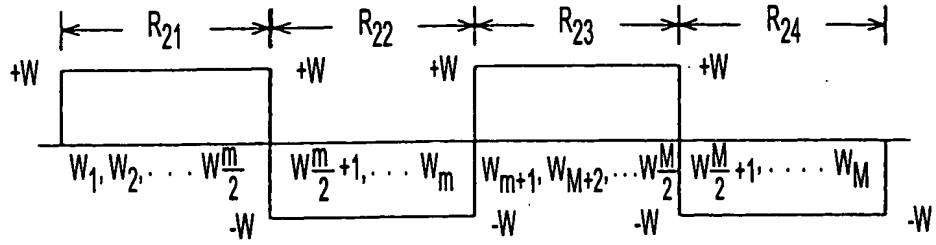

FIG. 9b

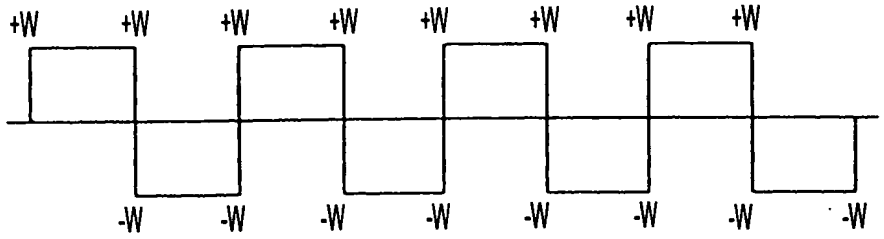

FIG. 9c

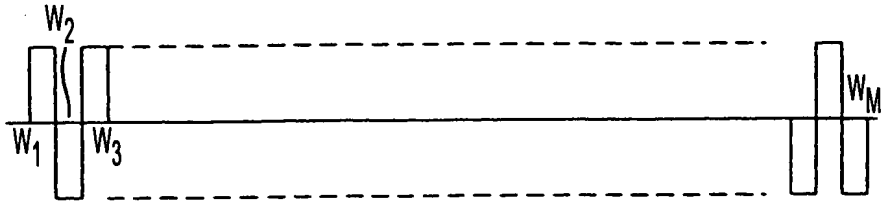

FIG. 9d

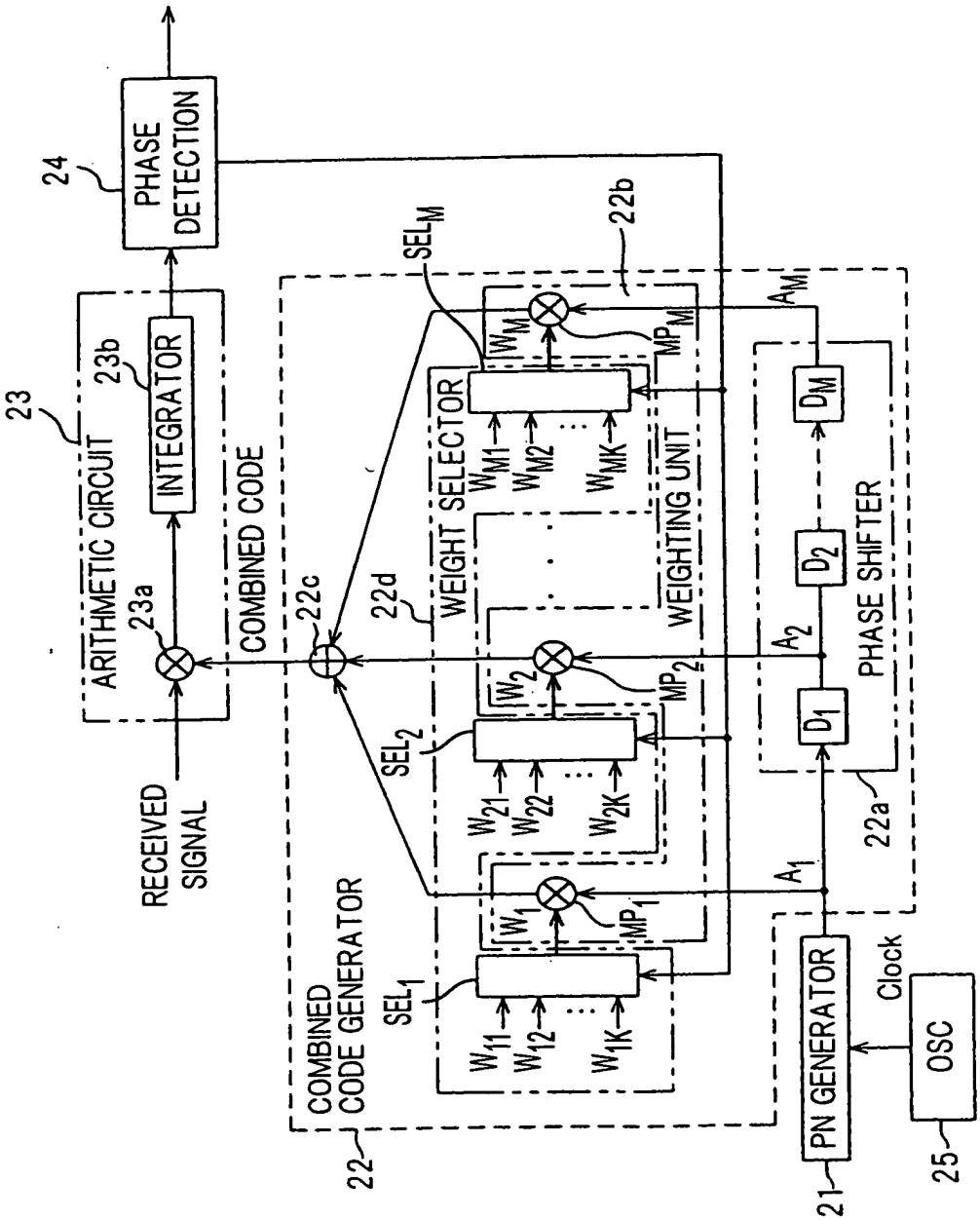
24
PHASE DETECTION
23
ARITHMETIC CIRCUIT
23b
INTEGRATOR
23a
COMBINED CODE
RECEIVED SIGNAL
22c
22d
WEIGHT SELECTOR
WEIGHTING UNIT
22b
SEL_M
W_M
MP_M
A_M
D_M
W_M1
W_M2
W_MK
D_2
A_2
MP_2
W_2
SEL_2
W_21
W_22
W_2K
D_1
PHASE SHIFTER
22a
A_1
MP_1
W_1
SEL_1
W_11
W_12
W_1K
COMBINED CODE GENERATOR
22
PN GENERATOR
21
Clock
OSC
25

FIG. 10

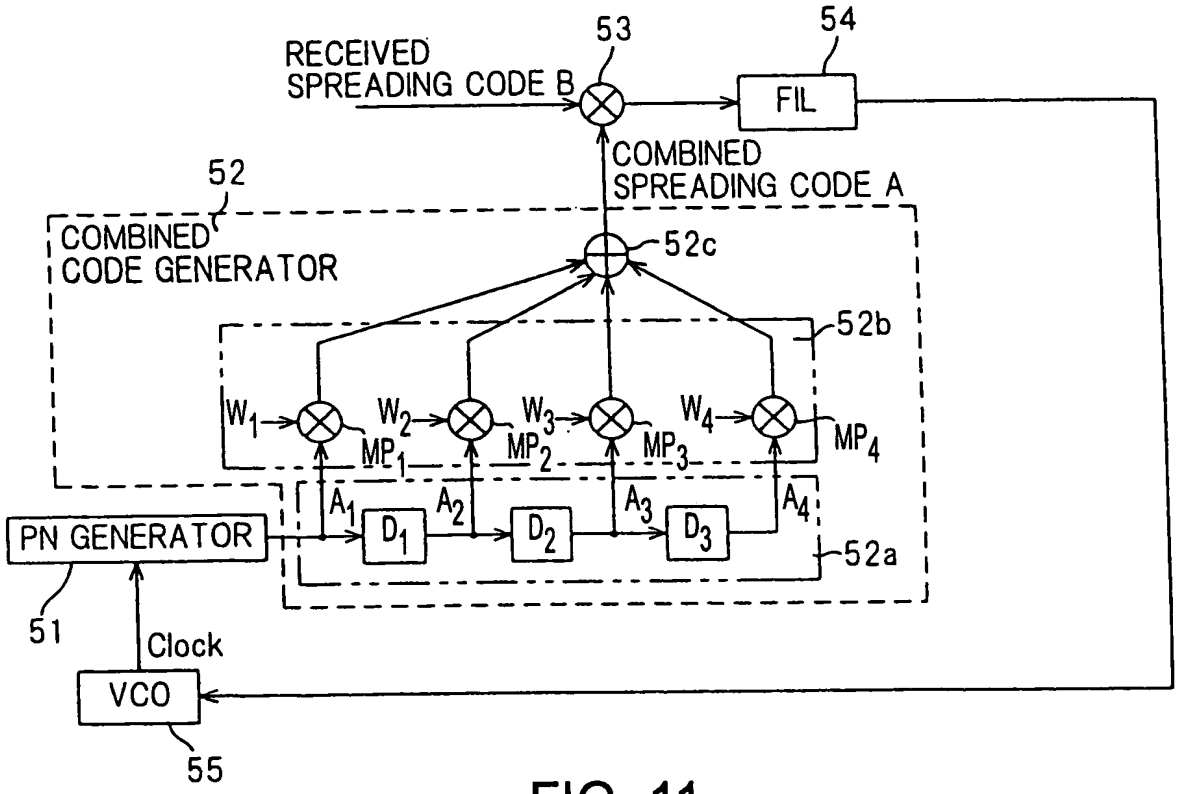
RECEIVED
SPREADING CODE B
53
54
FIL
COMBINED
SPREADING CODE A
52
COMBINED
CODE GENERATOR
52c
52b
W1
W2
W3
W4
MP1
MP2
MP3
MP4
A1
A2
A3
A4
D1
D2
D3
PN GENERATOR
52a
51
Clock
VCO
55

FIG. 11

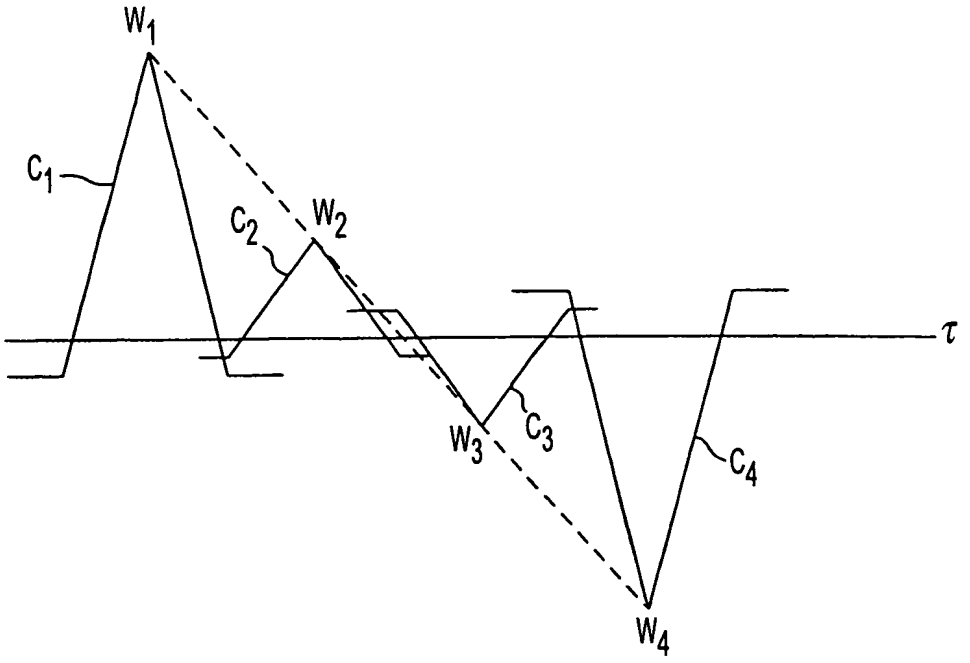

FIG. 12

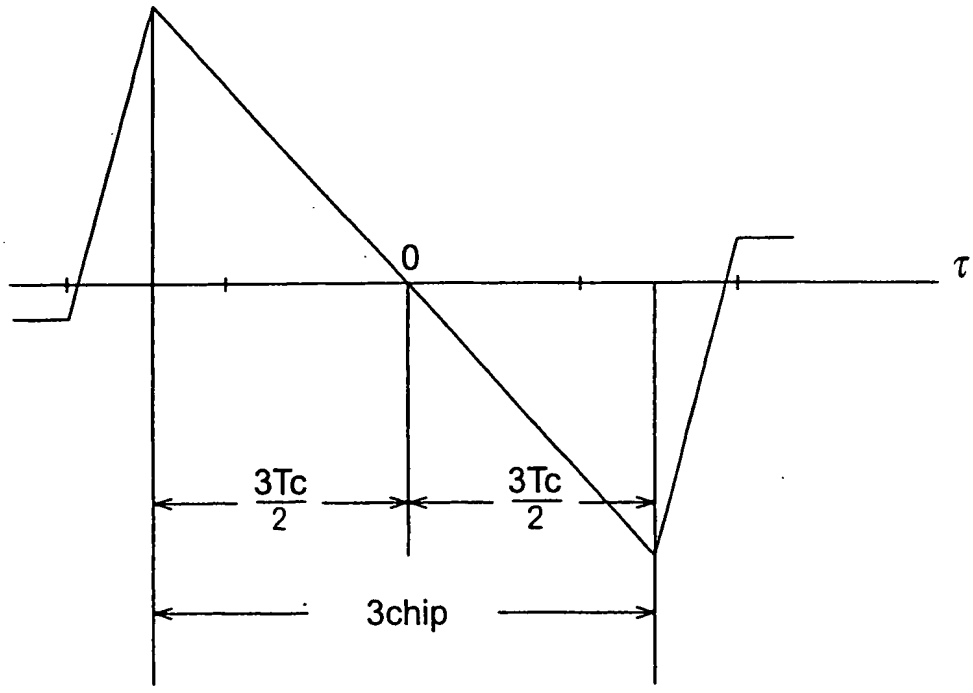

FIG. 13

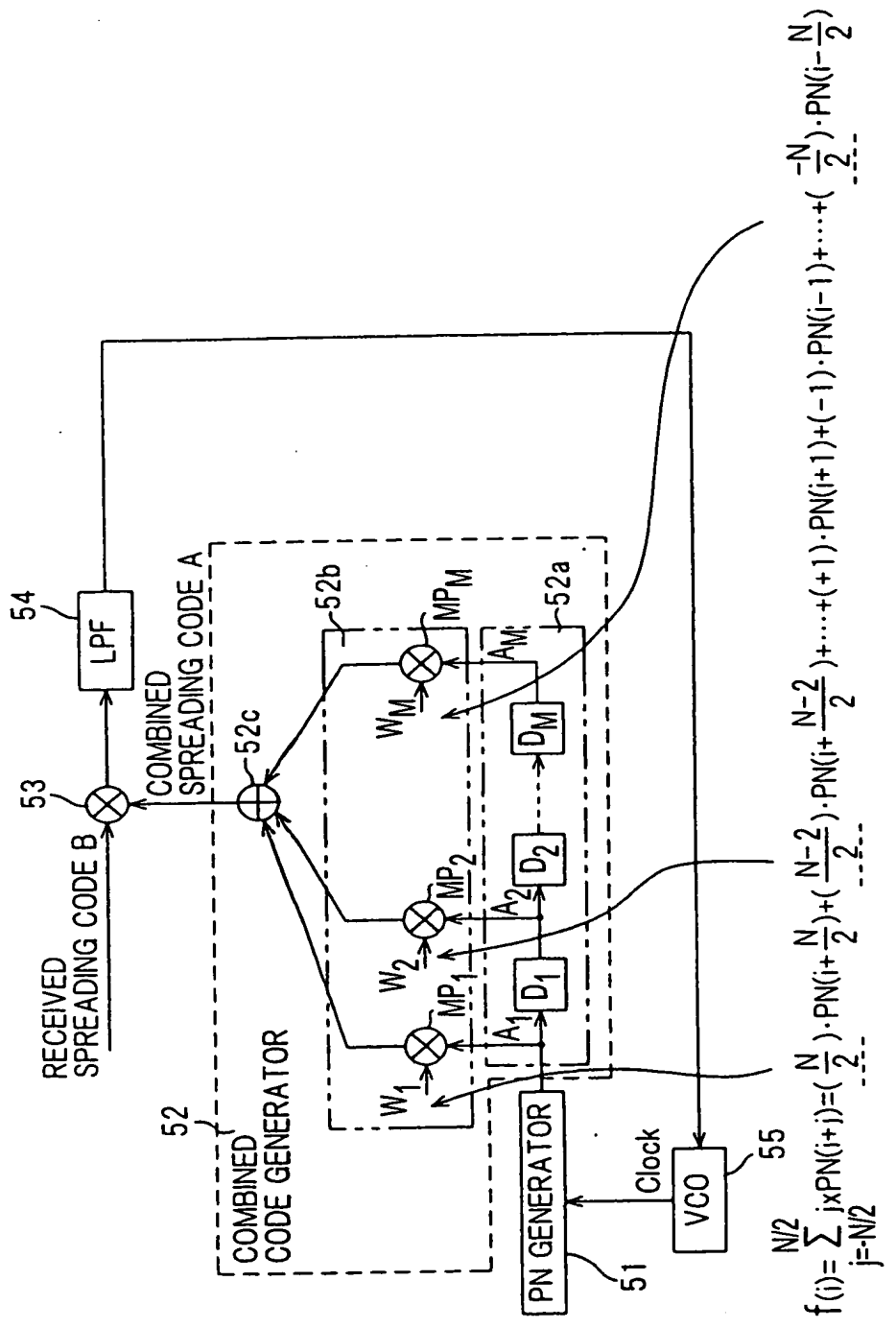
RECEIVED SPREADING CODE B
53
54
LPF
COMBINED SPREADING CODE A
52
COMBINED CODE GENERATOR
52c
52b
52a
W_1
W_2
W_M
MP_1
MP_2
MP_M
A_1
A_2
A_M
D_1
D_2
D_M
PN GENERATOR
51
Clock
VCO
55
$f(i)=\sum_{j=-N/2}^{N/2} jxPN(i+j)=(\frac{N}{2})\cdot PN(i+\frac{N}{2})+(\frac{N-2}{2})\cdot PN(i+\frac{N-2}{2})+\cdots+(+1)\cdot PN(i+1)+(-1)\cdot PN(i-1)+\cdots+(\frac{-N}{2})\cdot PN(i-\frac{N}{2})$

FIG. 14

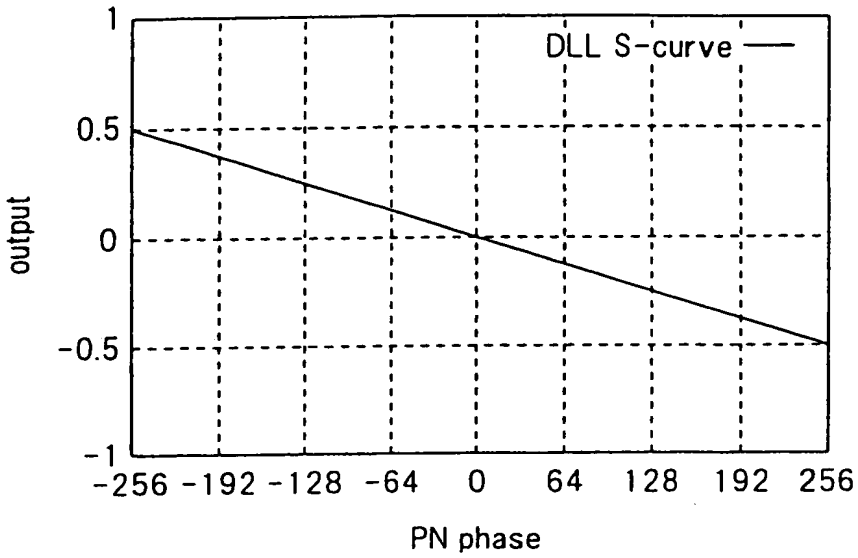
DLL S-curve
1
0.5
0
-0.5
-1
output
-256 -192 -128 -64 0 64 128 192 256
PN phase

FIG. 15

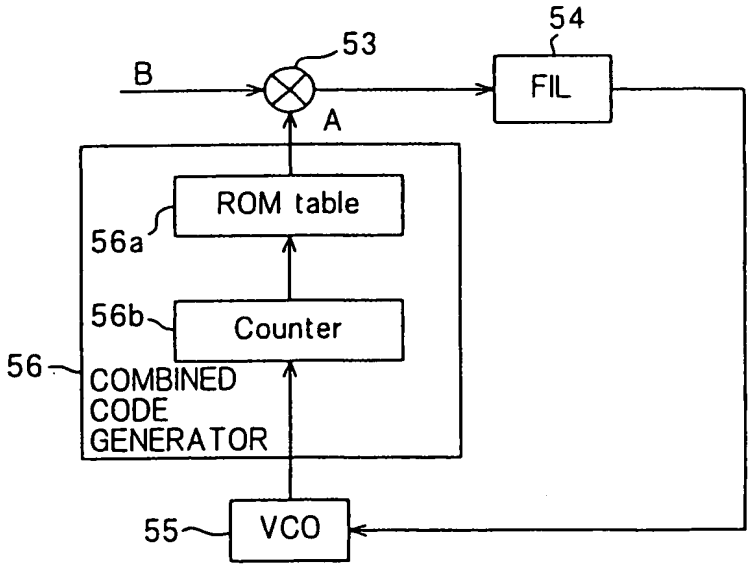
54
53
B
FIL
A
ROM table
56a
56b
Counter
56
COMBINED
CODE
GENERATOR
55
VCO

FIG. 16

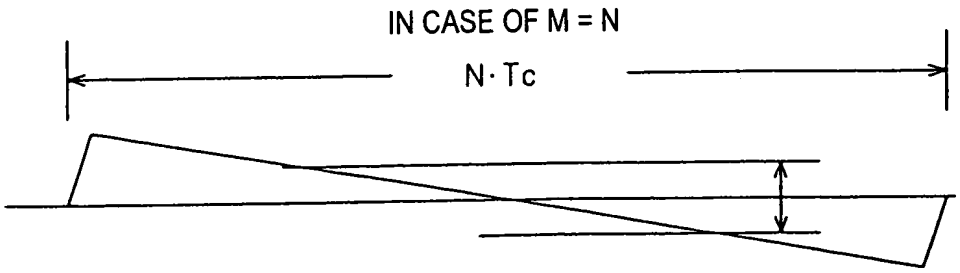

FIG. 17a

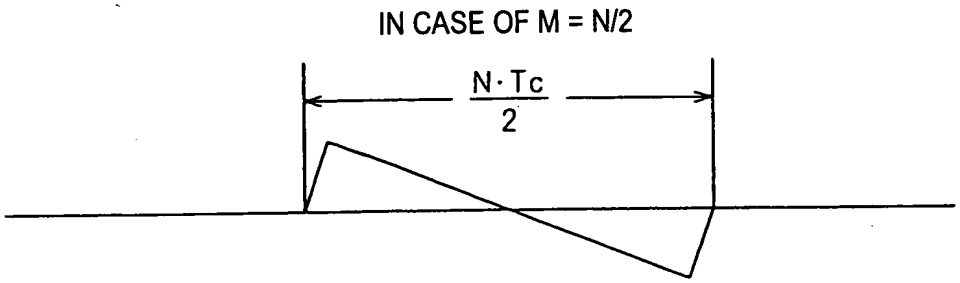

FIG. 17b

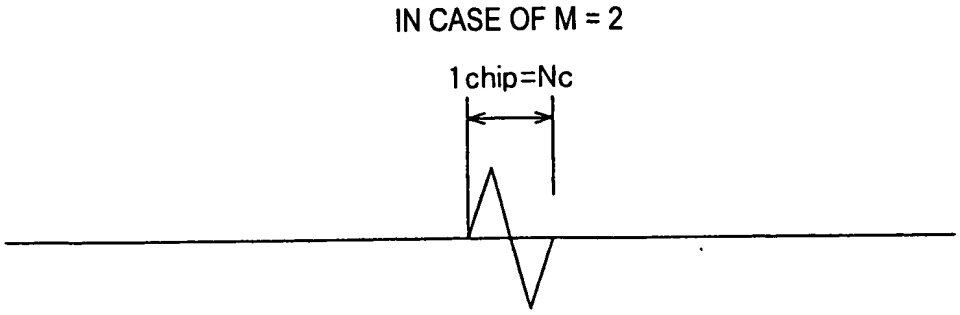

FIG. 17c

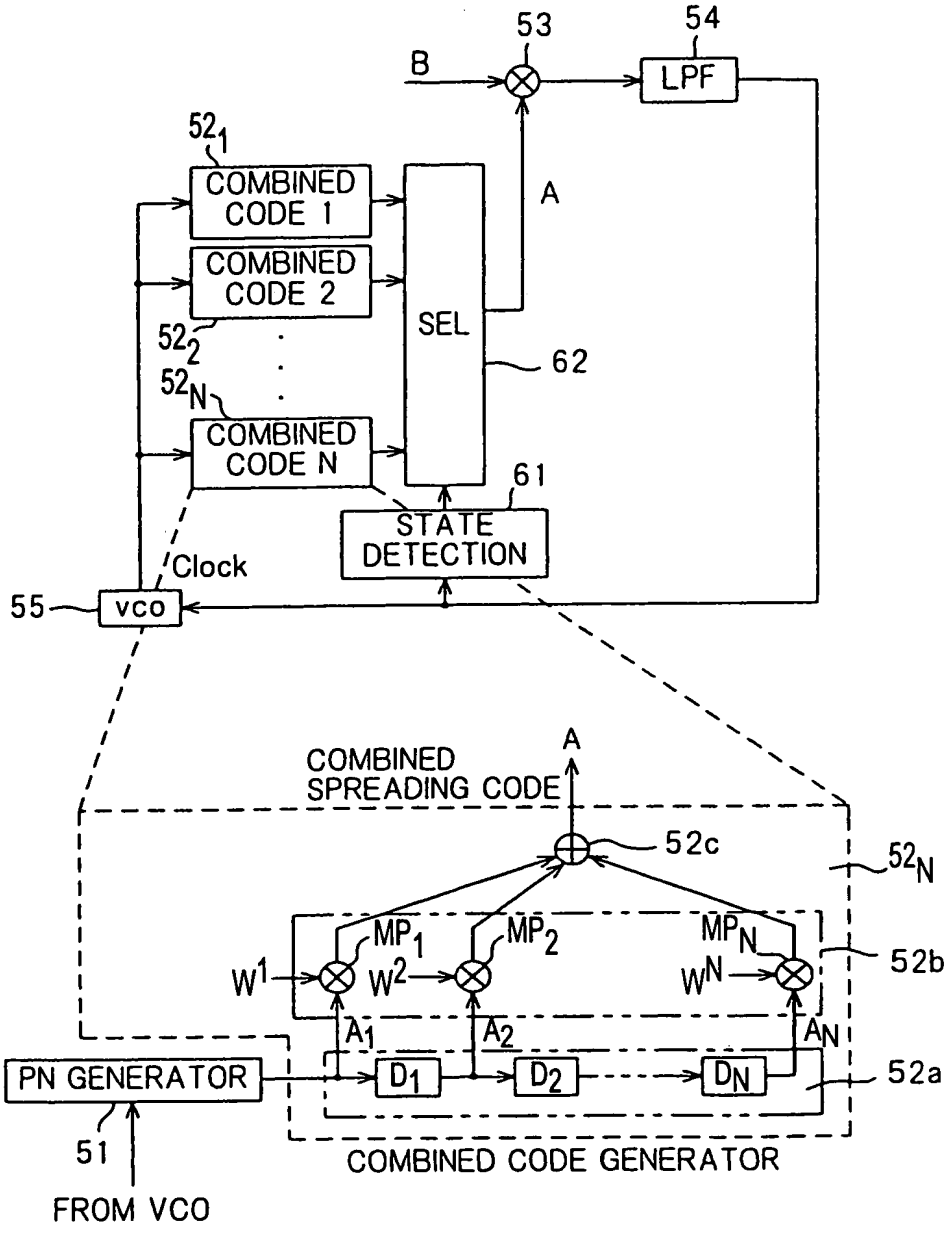
B
53
54
LPF
52_1
COMBINED CODE 1
COMBINED CODE 2
52_2
52_N
COMBINED CODE N
SEL
A
62
61
STATE DETECTION
Clock
55
VCO
COMBINED SPREADING CODE
A
52c
52_N
MP_1
MP_2
MP_N
W^1
W^2
W^N
52b
A_1
A_2
A_N
PN GENERATOR
D_1
D_2
D_N
52a
51
FROM VCO
COMBINED CODE GENERATOR

FIG. 18

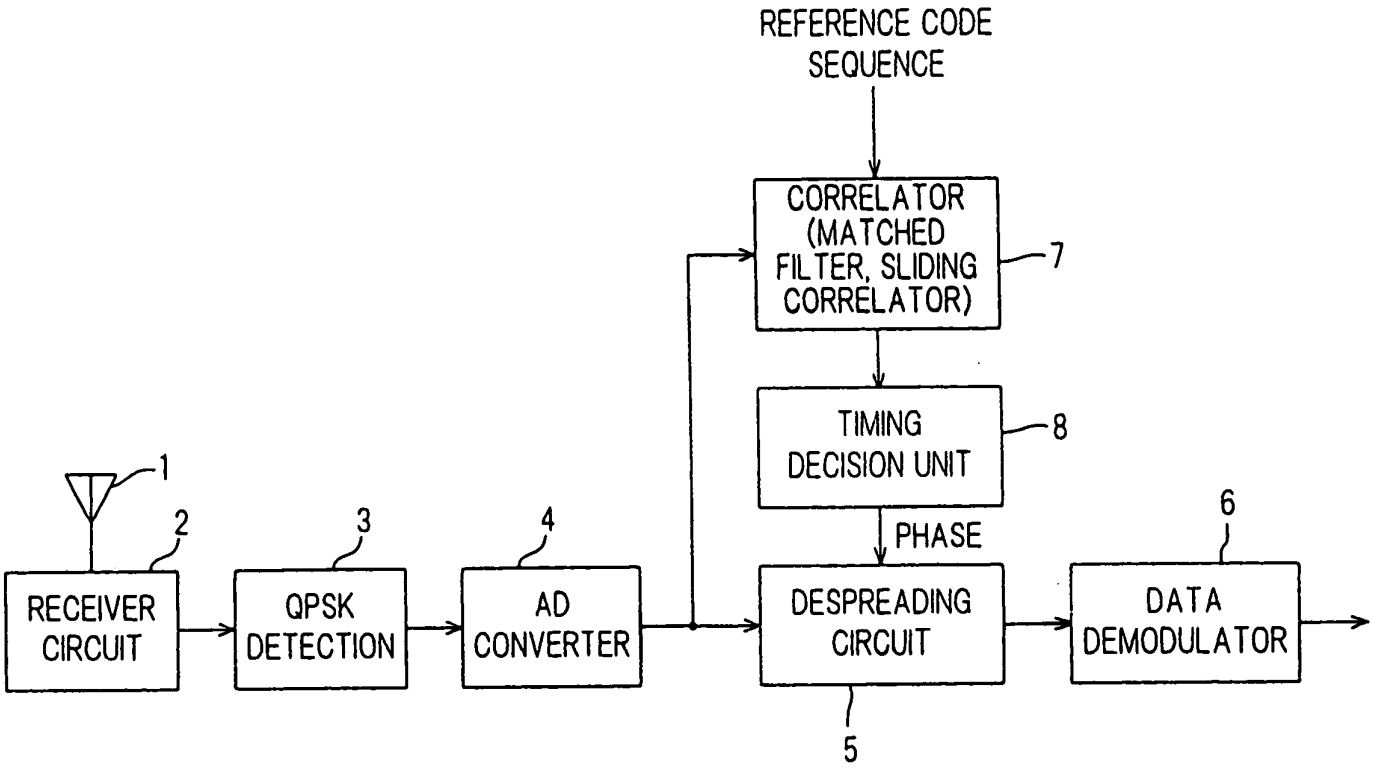

FIG. 19
(PRIOR ART)

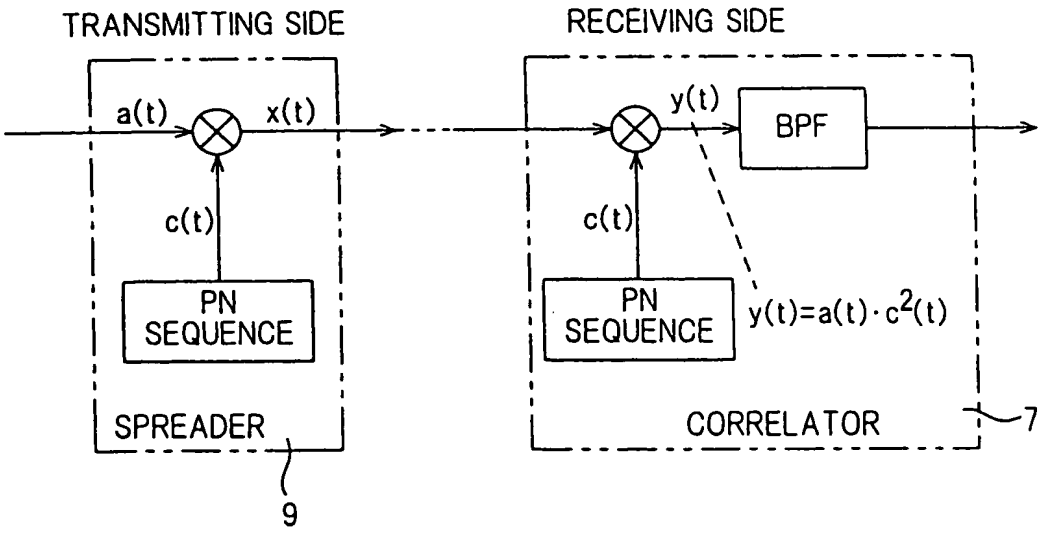

FIG. 20
(PRIOR ART)

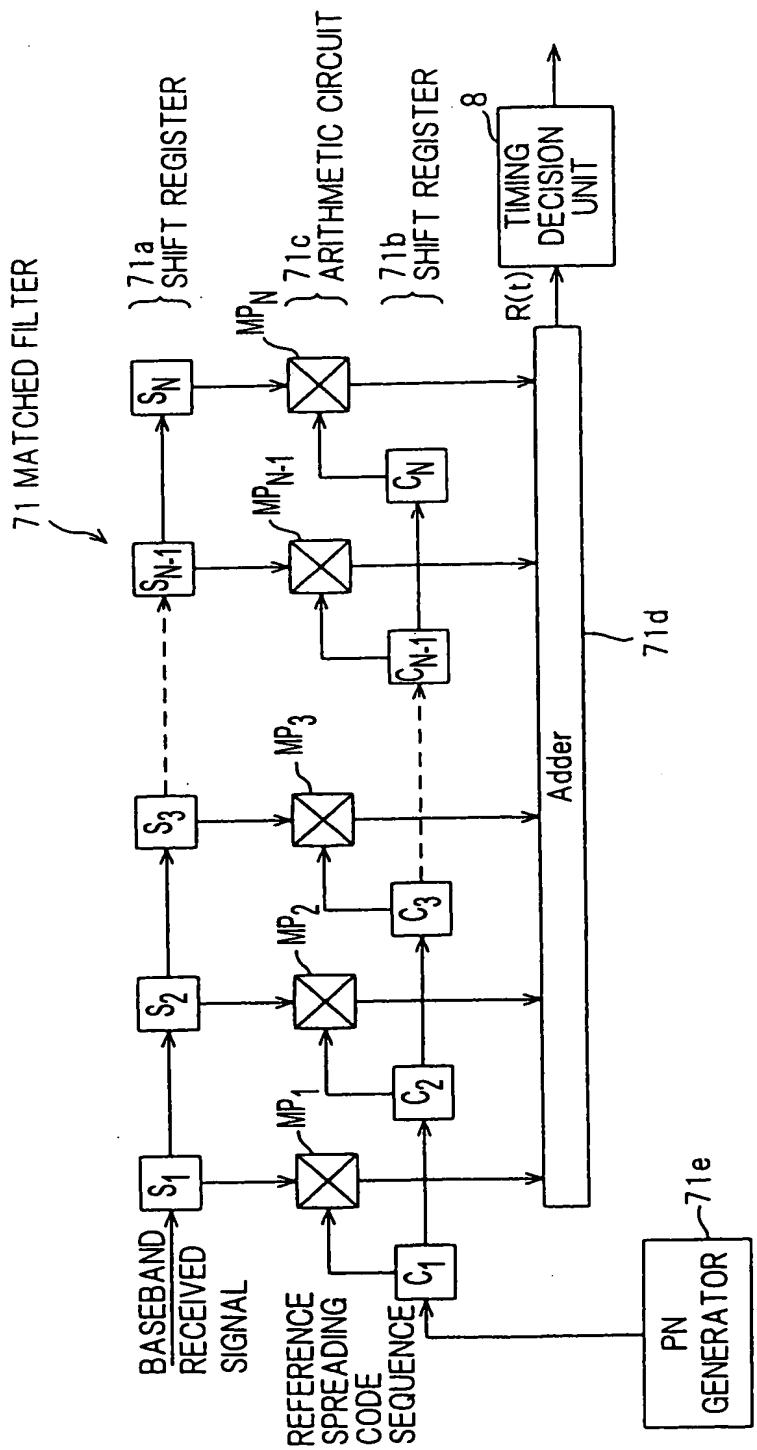
71 MATCHED FILTER
71a SHIFT REGISTER
71c ARITHMETIC CIRCUIT
71b SHIFT REGISTER
8
TIMING DECISION UNIT
R(t)
BASEBAND RECEIVED SIGNAL
REFERENCE SPREADING CODE SEQUENCE
PN GENERATOR
71e
Adder
71d
S1
S2
S3
SN-1
SN
C1
C2
C3
CN-1
CN
MP1
MP2
MP3
MPN-1
MPN

FIG. 21

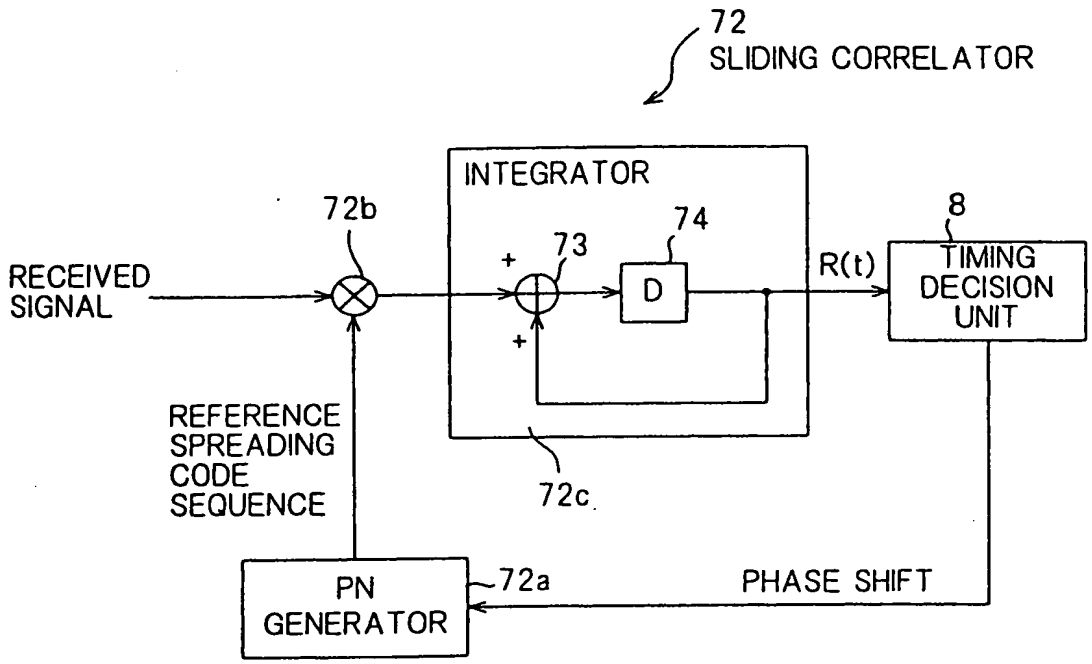
72
SLIDING CORRELATOR
INTEGRATOR
72b
73
74
8
RECEIVED SIGNAL
+
+
D
R(t)
TIMING DECISION UNIT
REFERENCE SPREADING CODE SEQUENCE
72c
PN GENERATOR
72a
PHASE SHIFT

FIG. 22

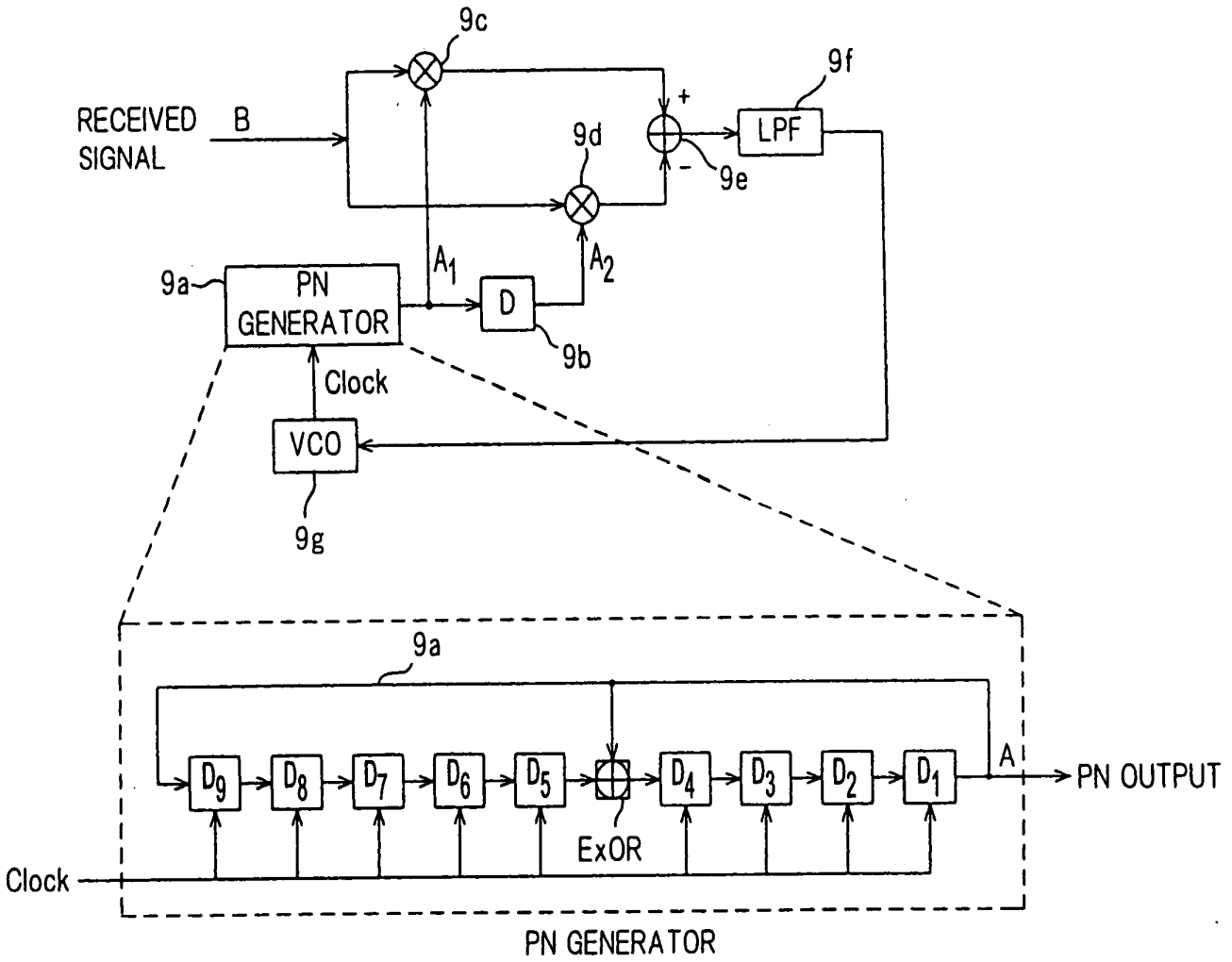

FIG. 23
(PRIOR ART)

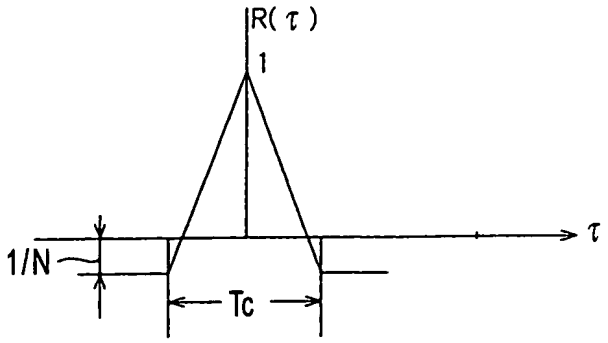

FIG. 24a
(PRIOR ART)

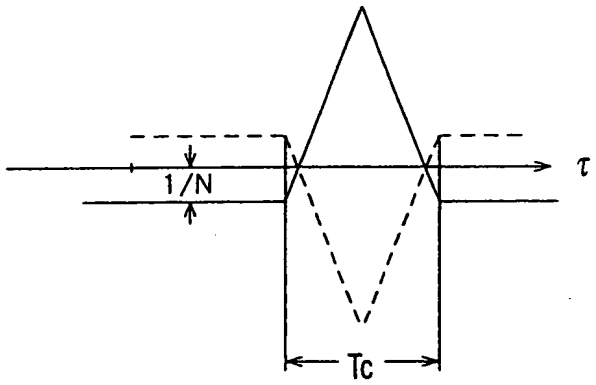

FIG. 24b
(PRIOR ART)

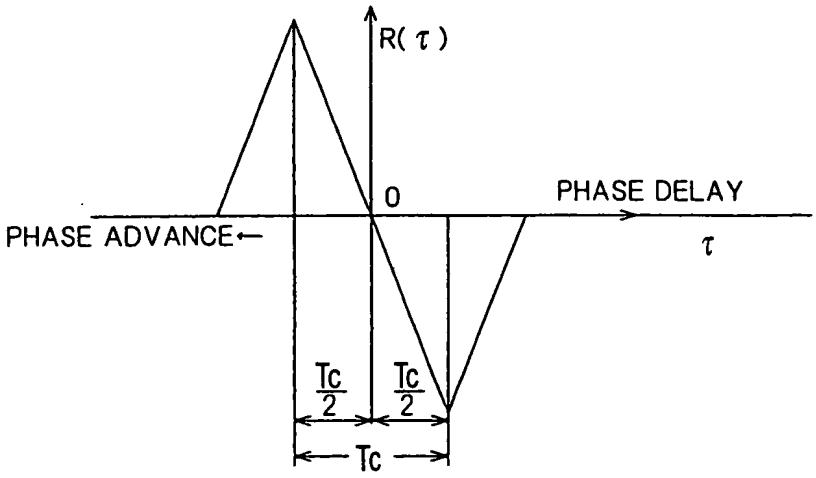

FIG. 24c
(PRIOR ART)

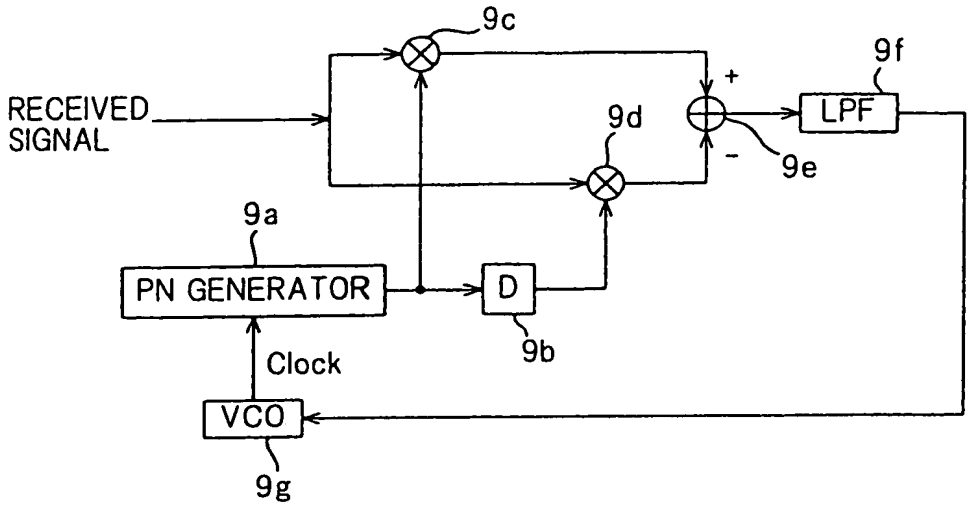

FIG. 25a
(PRIOR ART)

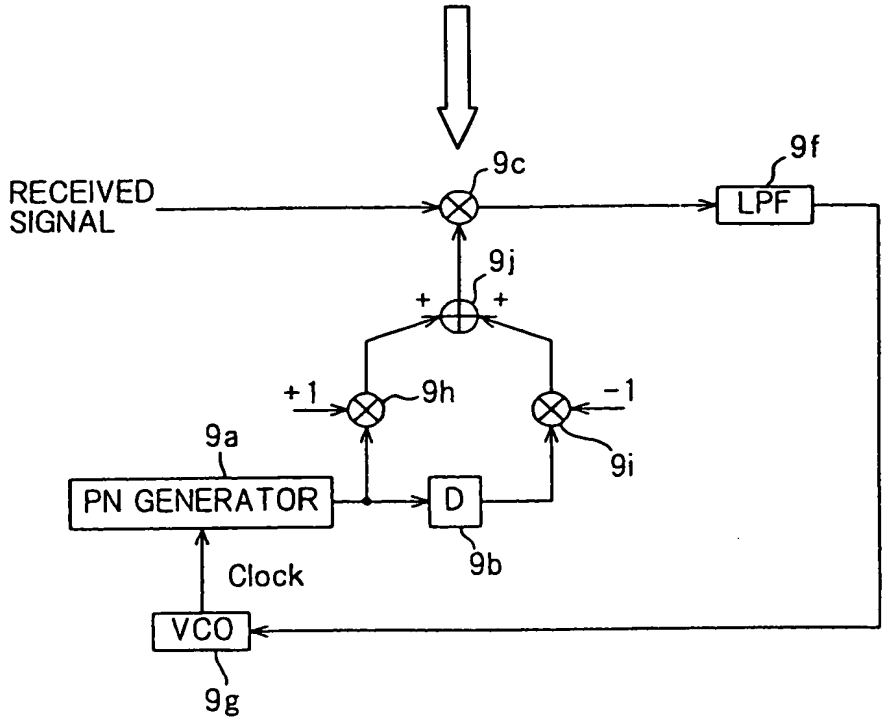

FIG. 25b
(PRIOR ART)